R&D of Integrated Detector Readout

DOE OHEP Comparative Laboratory Review of Generic R&D

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U.S. DEPARTMENT OF ENERGY | Office of Science

Outline

- Introduction
- R&D of Integrated Solutions for Detector Readout
  - Past Achievements
  - Ongoing Work
  - Future Plans
- Collaboration with Universities
- Resources & Budget
- Conclusion

Introduction (1)

- R&D at BNL has been focused on the overall system optimization for experiments
  - Initiated by physics motivation, start from detector & readout development, to trigger and DAQ implementation
  - ***R&D started on generic idea & technology, gradually evolved into customized solution for various particular experiments***
  - Great leverage of expertise available in Physics Department and Instrumentation Division, covering various areas, from detector, readout to trigger and DAQ
- ***Goals of R&D: Continuously develop expertise in select sensor and electronics technologies, aimed to efficiently provide integrated solutions of Readout and Trigger/DAQ systems for future experiments***
  - Noble Liquid TPCs for Neutrino Experiments:
    Low Noise Multiplexed Readout integrated on the TPC electrodes
  - Hadron Collider Experiment: ATLAS Detector Upgrade
  - ***See S. Li's talk for ASIC Development***
  - ***See M. Begel's talk for R&D on trigger and DAQ***

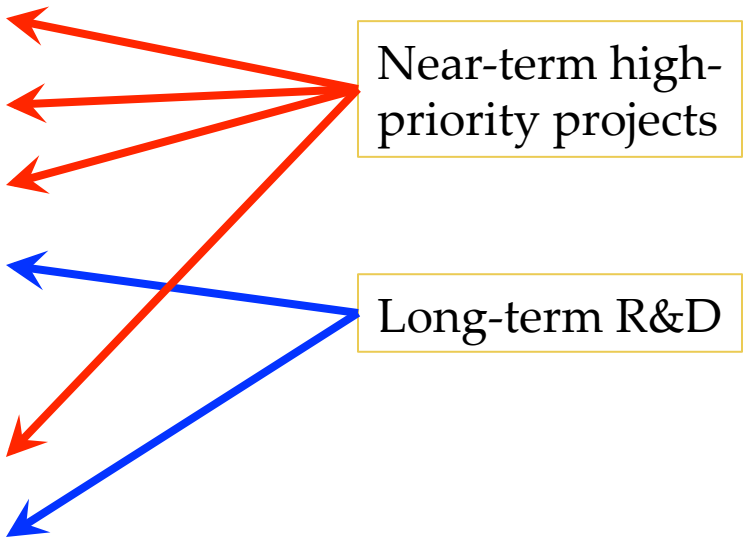
Introduction (2)

- The R&D of integrated detector readout at BNL has been following this trend and focused on the following two areas
  - ***Operation in noble liquids (e.g. LAr at ~89K)***
  - ***Operation in radiation environment at high collider luminosity***
- Front-end ASICs and boards design are being ***optimized for two distinctly different sets*** of experimental and environmental conditions
  - ***Cryogenic temperature, waveform recording at low rates, for noble liquid TPCs***
  - ***High counting rates, magnetic field and radiation for (HL-)LHC***

Introduction (3)

- *P5 recommendation 27: Focus resources toward directed instrumentation R&D in the near-term for high-priority projects. As the technical challenges of current high-priority projects are met, restore to the extent possible a balanced mix of short-term and long-term R&D*

- Intensity Frontier Experiments
  - MicroBooNE
  - SBND
  - ProtoDUNE
  - DUNE Far Detector
- Energy Frontier Experiments
  - ATLAS Phase-I Upgrade
  - ATLAS Phase-II Upgrade



R&D on Cold Electronics

- R&D of CMOS cold electronics started in 2008
  - Analog FE ASIC was the first one developed, following by ADC ASIC development, studies of cold regulator and FPGA etc.
  - In parallel, studies of CMOS lifetime and reliability at 77 K were conducted
    - *"LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," IEEE Trans. on NSci, 60, No: 6, Part: 2, p4737(2013)*
  - Gradually build up a full solution of cold front end readout electronics chain
  - ***Cold electronics development was done for the most part before the projects were formed and limited project funding became available***

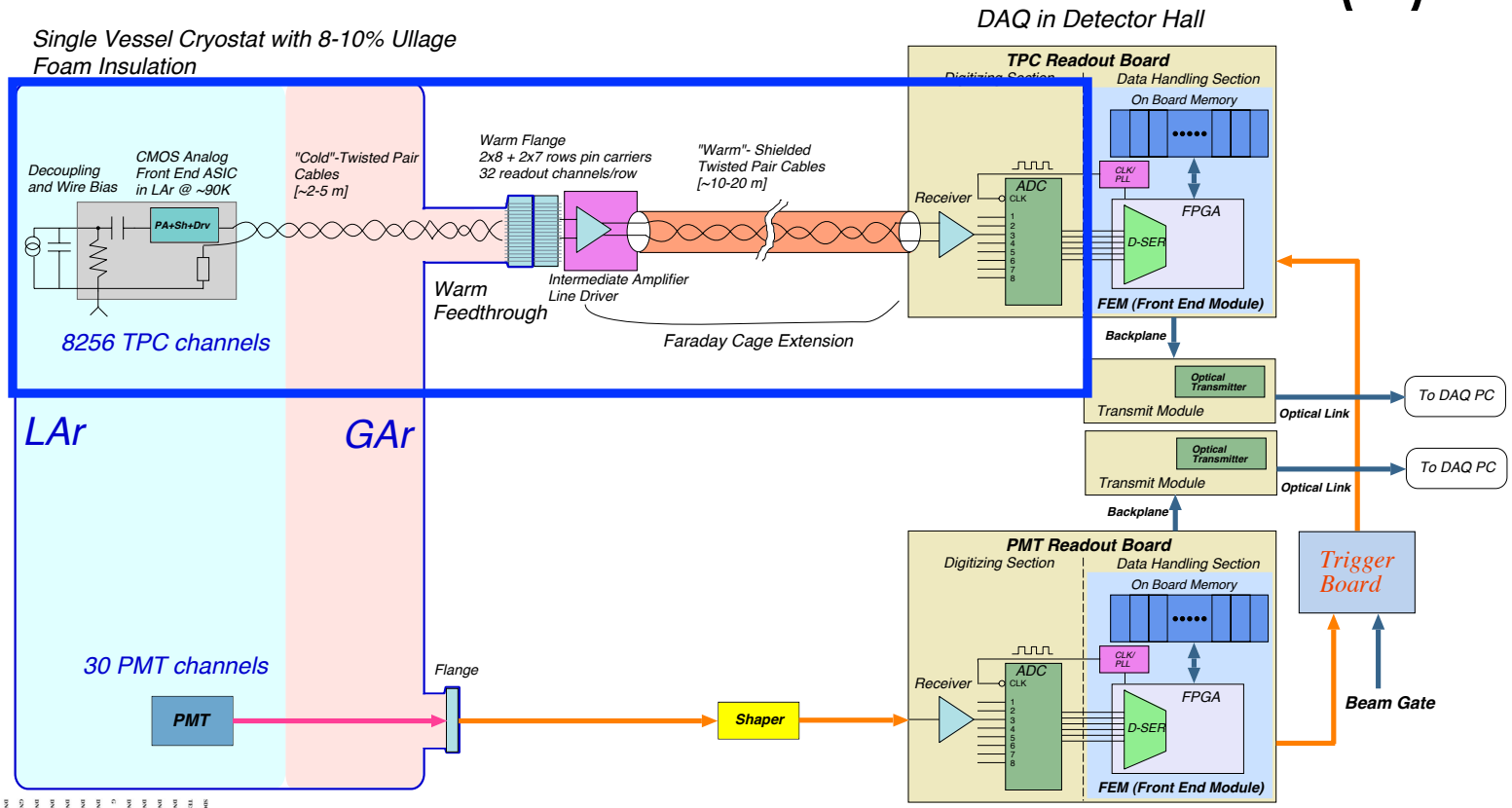
- Projects using, and potentially will be using cold electronics:
  - MicroBooNE
  - LArIAT
  - SBND
  - DUNE 35Ton
  - DUNE 10kt Far Detector
  - ARGONTUBE at Bern
  - ICARUS 50l TPC at CERN
  - ArgonCUBE at Bern
  - ProtoDUNE at CERN

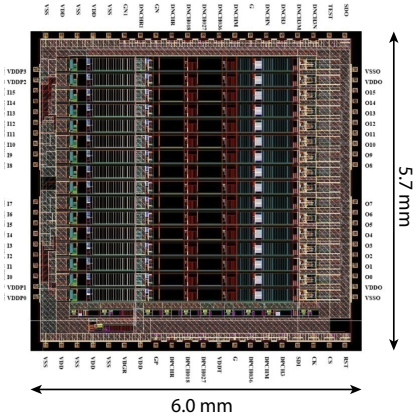
- ***R&D on cold electronics started before most of these projects were anticipated or in existence → an example of long term R&D with high return***

Past Achievements

- Neutrino Experiment
  - MicroBooNE is the first experiment using cold CMOS analog FE ASIC operating in LAr
- ***An example of evolution from generic R&D to experiment***
  - Core experts are supported by KA25 & Instrumentation, which leads to a project successfully
  - Further development for experiments is supported by project

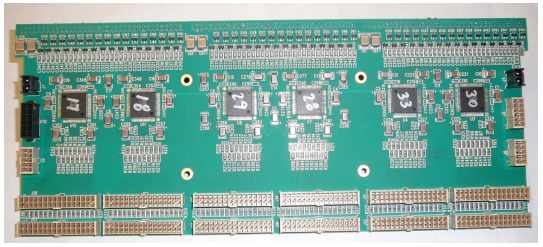
MicroBooNE Front End Electronics (1)

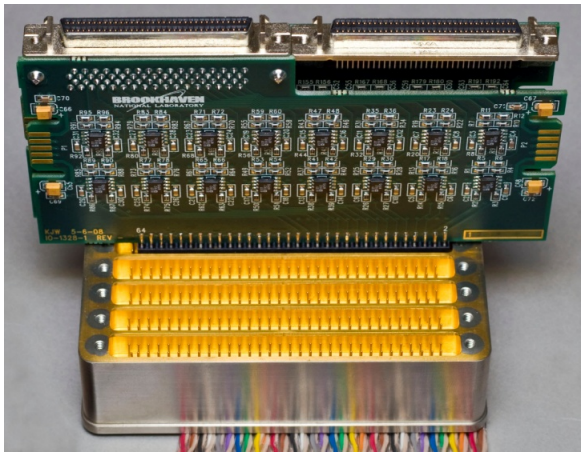


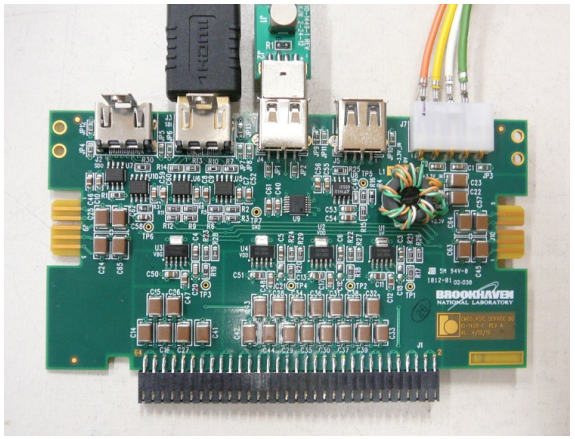


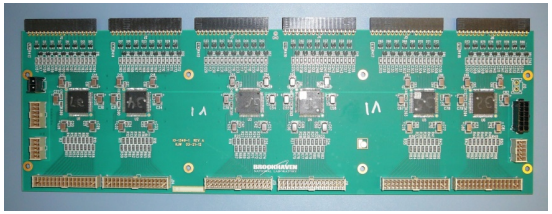
- BNL designed front end readout electronics system for MicroBooNE experiment
- Analog front-end ASIC designed in 180 nm is running in LAr (~89 K) to achieve optimum signal to noise ratio
- MicroBooNE is the first experiment instrumented with cold CMOS ASICs

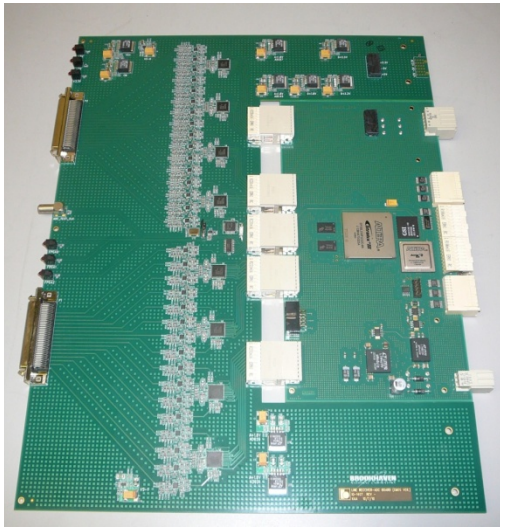
MicroBooNE Front End Electronics (2)

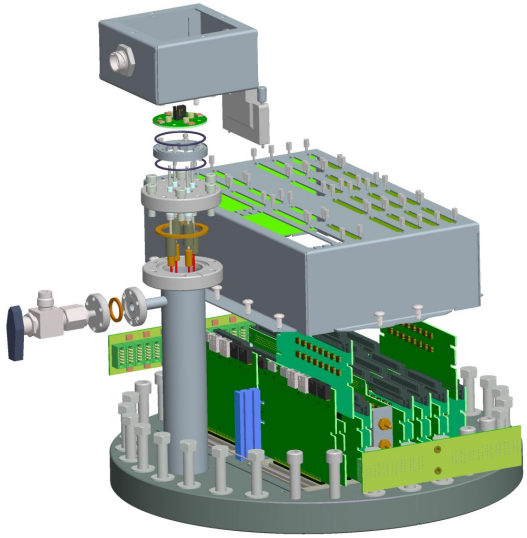




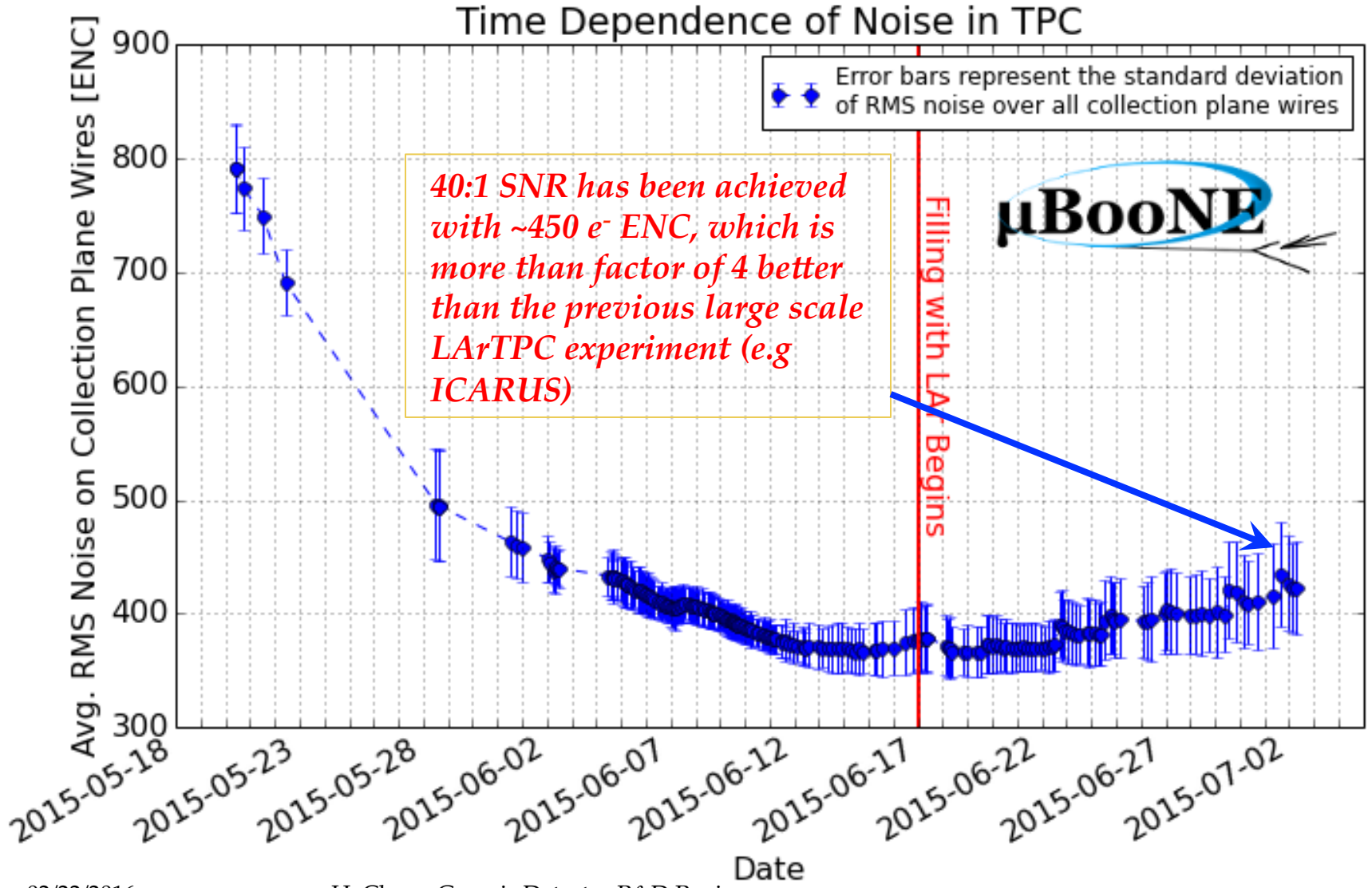








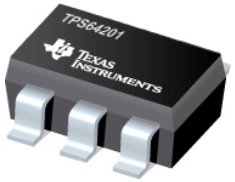
MicroBooNE Cold Electronics Temperature Dependence of Noise in TPC



On Going Work

- Neutrino Experiment
  - SBND
  - ProtoDUNE
  - ***Both SBND & protoDUNE will use the next generation of CMOS cold electronics, including analog FE ASIC, ADC ASIC and FPGA, all operating in LAr***
  - ***Advancement of generic R&D enables the evolution of readout solution for neutrino experiments***
- Hadron Collider Experiment
  - ATLAS Phase-I Upgrade
  - ***VMM ASIC is a SoC (System on Chip) developed for Muon NSW (New Small Wheel)***

Cold Electronics

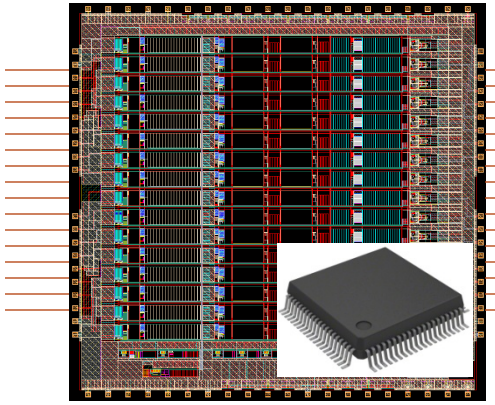


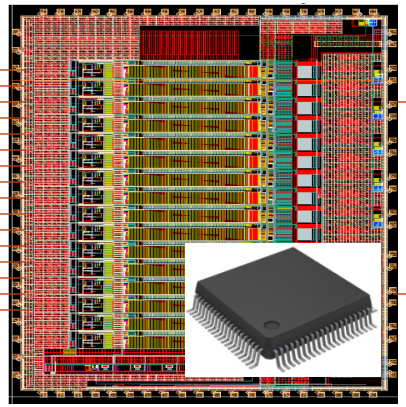
voltage regulation
(COTS)
(< 100mV dropout)

front-end ASIC
~ 5mW/ch.

ADC ASIC
~ 5mW/ch.

FPGA (COTS)
~ 8mW/ch.



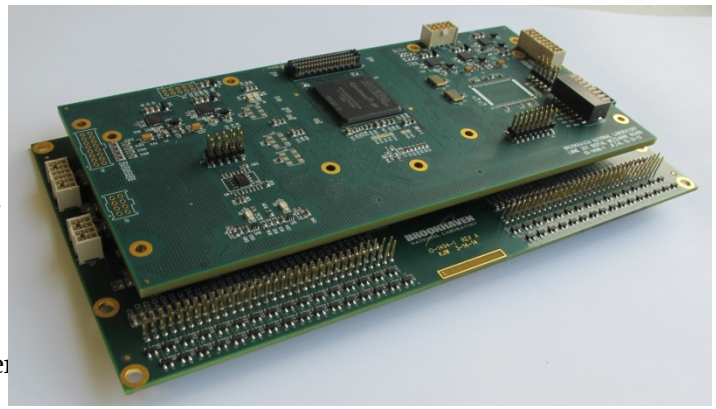


overall 128:4
multiplexing

8 x

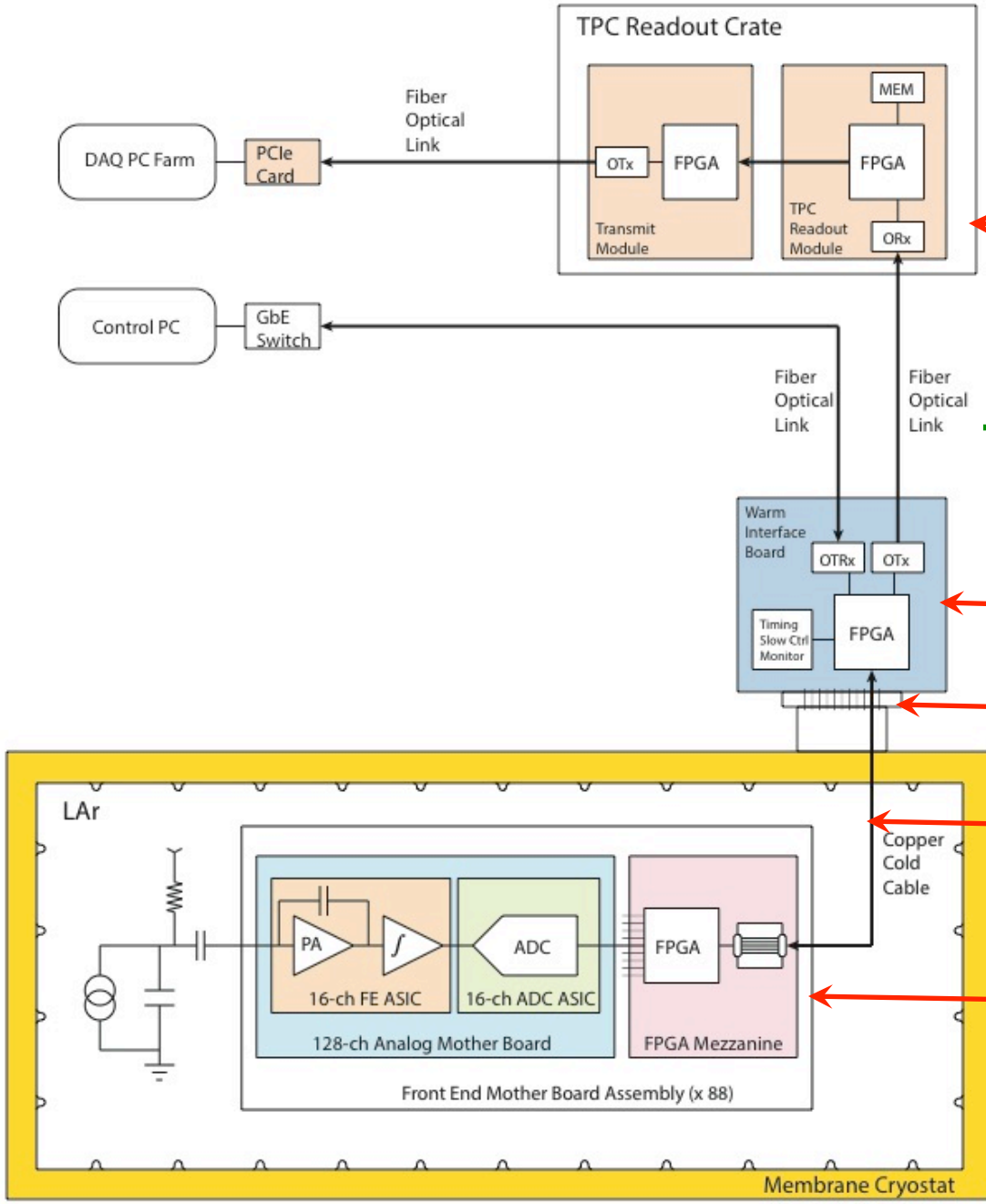
1 x

A Complete Front End Readout Chain for SBND & protoDUNE



front-end mother
board assembly
serving 128 wires
~ 2.4 W

SBND TPC Electronics



TPC Readout Electronics

Back End Electronics

Front End Electronics

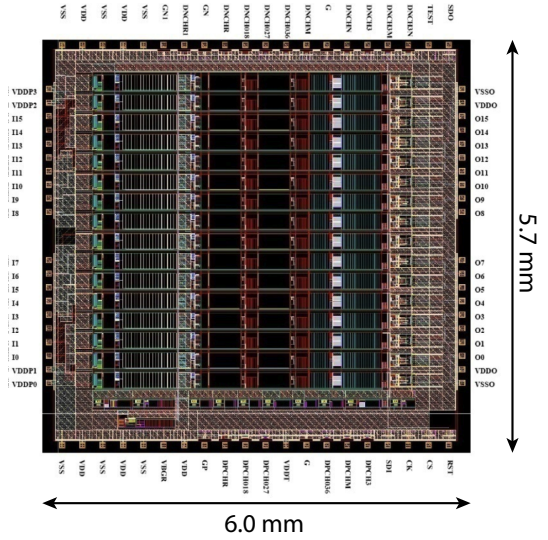
Warm Interface Electronics

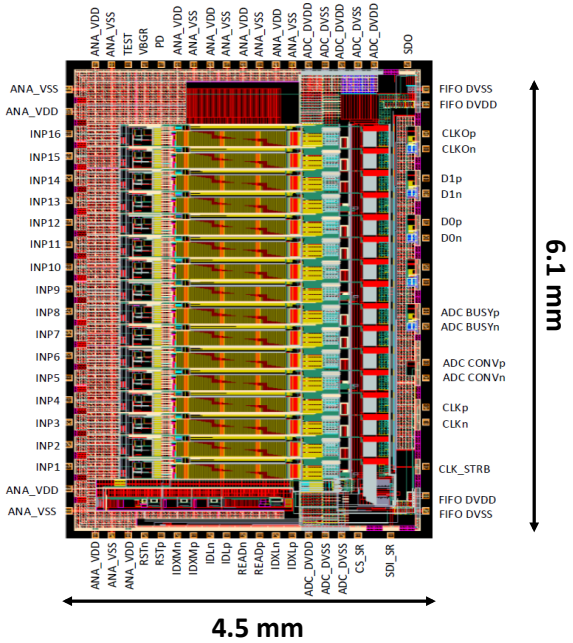
Signal Feed-through

Cold Cable

Cold Electronics

Advancement of Cold ASICs Design

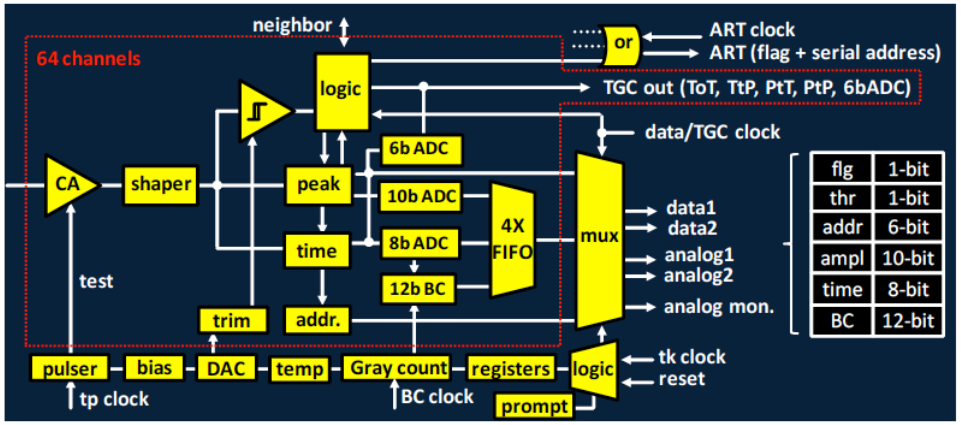


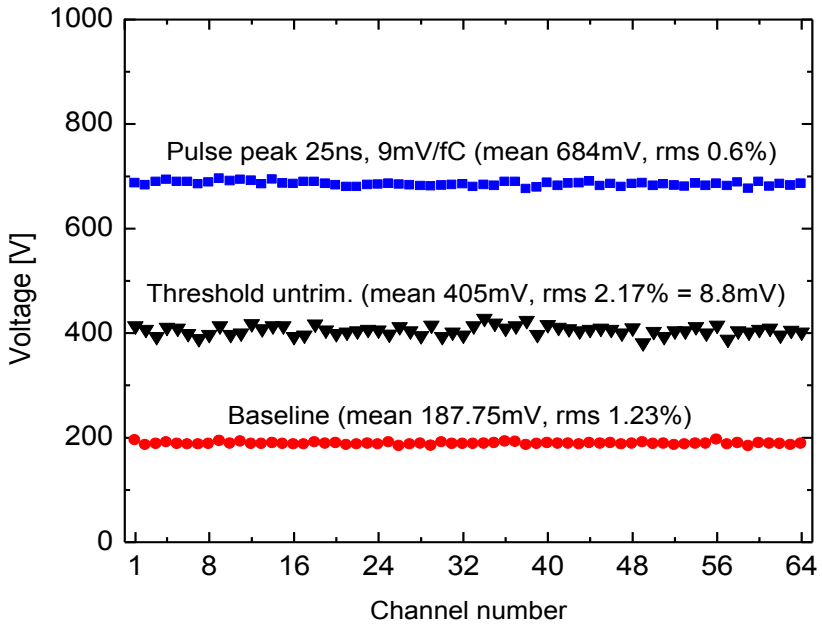


- Further development of cold FE & ADC ASICs aim to further improve the robustness of chip and simplify the system design of the front end readout electronics
  - FE ASIC will have built in pulse generator for precision charge calibration
  - ADC ASIC will have simplified interface and improved performance to ease the usage in both small scale and multi-kton LAr TPC
- Both SBND at Fermilab and protoDUNE at CERN will use new cold ASICs to instrument the front end readout for LAr TPC

- SBND @ Fermilab
  - 11,264 channels
  - 704 FE ASICs/704 ADC ASICs/88 Cold FPGAs
  - 88 Front End Mother Board assemblies
  - 4 sets of cold cable bundles
  - 4 sets of signal feed-throughs
  - ~30 warm interface boards
- protoDUNE @ CERN
  - 15,360 channels
  - 960 FE ASICs/960 ADC ASICs/120 cold FPGAs
  - 120 Front End Mother Board assemblies
  - 8 sets of cold cable bundles
  - 8 sets of signal feed-throughs

Front-end ASIC for Muon New Small Wheel (1)





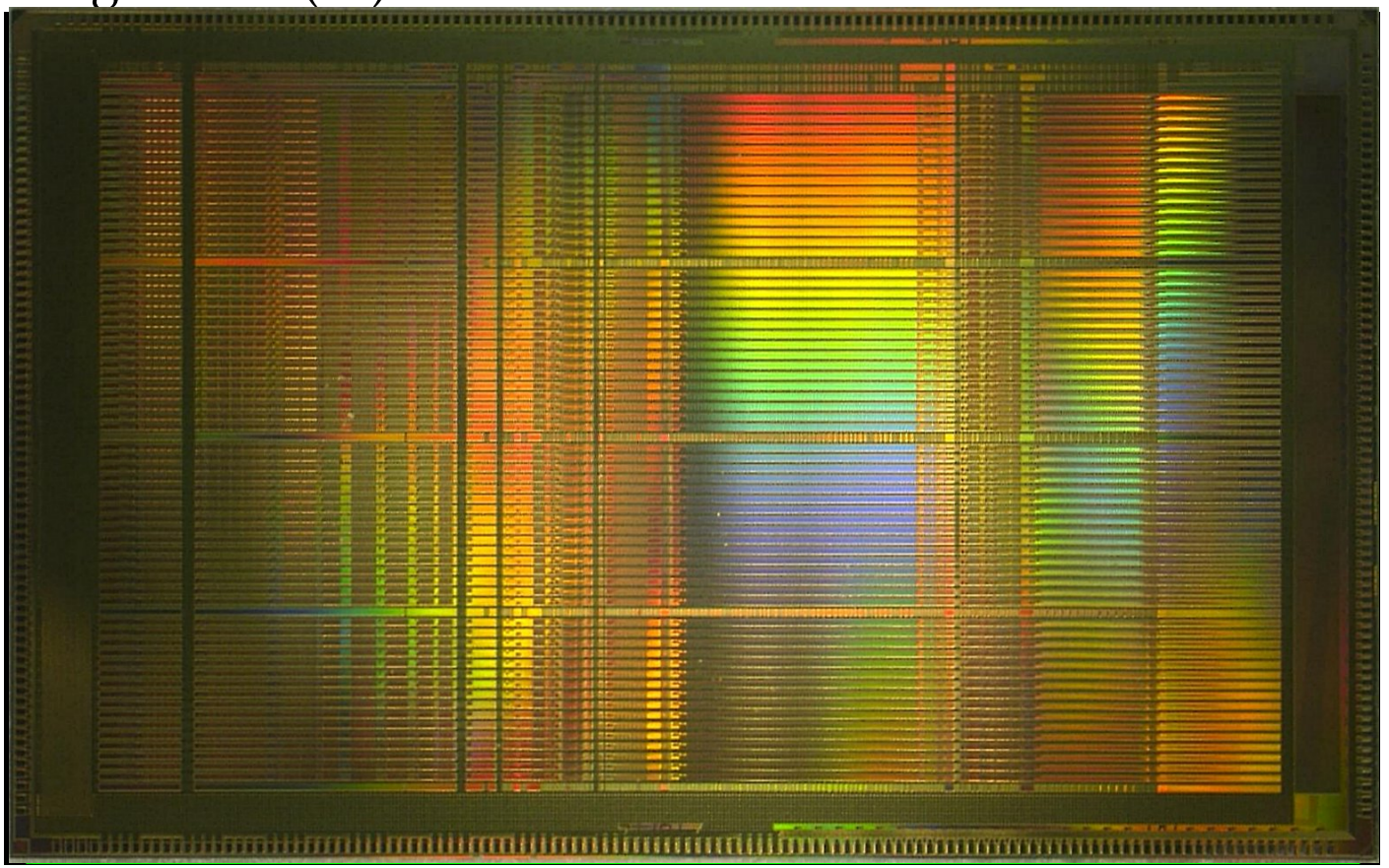
- VMM Chip
  - Versatile front-end ASIC for micro-pattern gas detectors
  - Suitable to both MicroMegas and sTGC in Muon NSW
  - Mixed-signal design, handle both signal polarities
  - 64 channels with integrated
    - 10-bit ADC per channel for peak amplitude measurement (multiplexed)
    - 8-bit ADC per channel for sub-nanosecond time measurement (multiplexed)
    - 6-bit FADC (25 ns conversion), 64 channel parallel output for trigger
    - Address of hit channel in real time (Fast OR with address) can also be used in trigger
  - Low power, 4-8 mW/channel depending on features used
  - CMOS 130 nm, 13.5 x 8.3 mm^2, over 5 million transistors
  - Excellent performance on VMM1 & VMM2, VMM3 submission will be in March

Front-end ASIC for Muon New Small Wheel (2)

- Layout and Packaging

analog, mixed-signal, digital supplies (1.2V) – neighbor.top
– digital IOs (14) - TGC outs 0-6

64 inputs, 9 preamplifier supply (1.2V)



TGC outs 7-42

analog, mixed-signal, digital supplies (1.2V) – neighbor.bottom
– TGC outs 43-63

13.5 mm

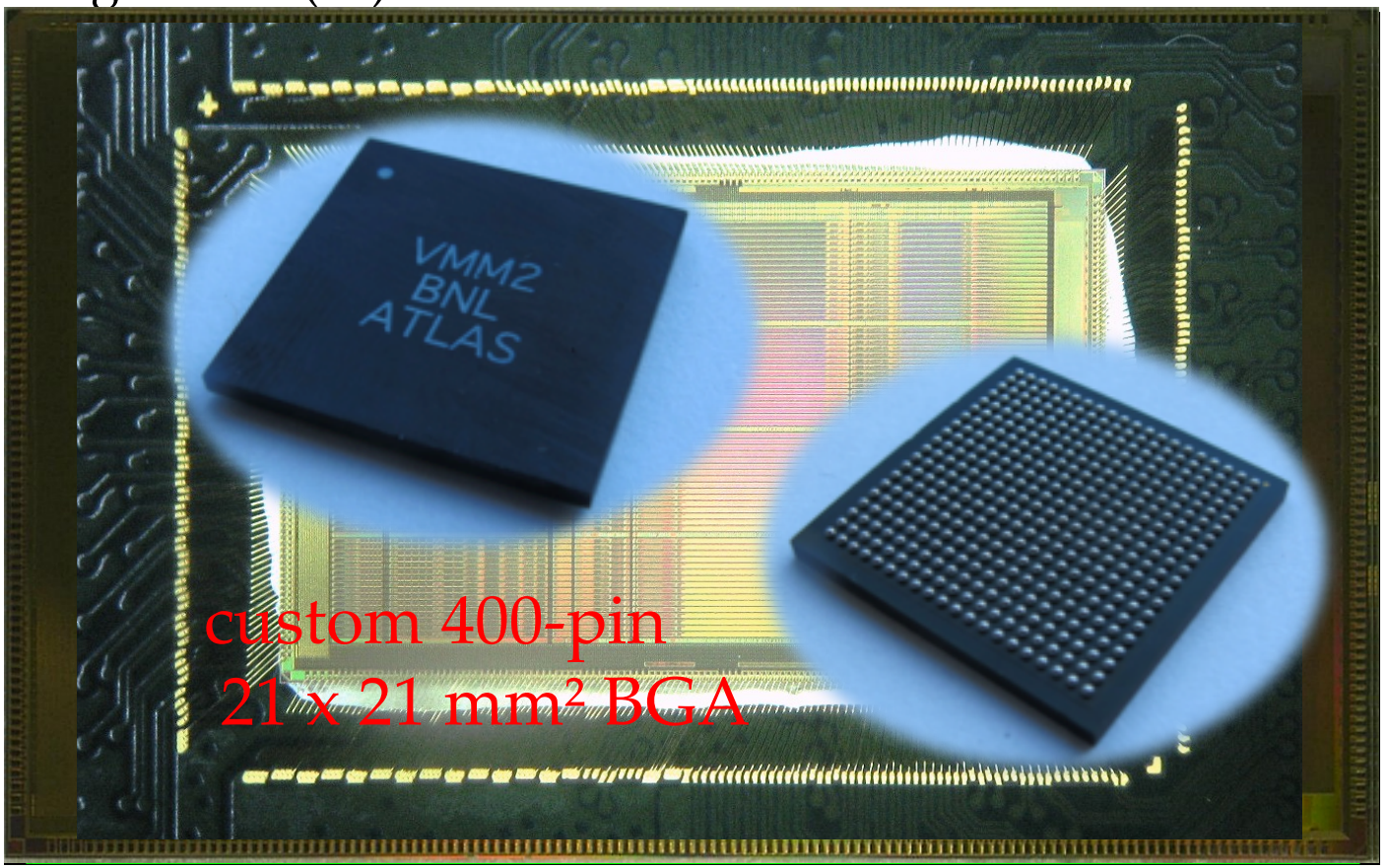
392 bonding pads

Front-end ASIC for Muon New Small Wheel (3)

- Layout and Packaging

analog, mixed-signal, digital supplies (1.2V) – neighbor.top
– digital IOs (14) - TGC outs 0-6

64 inputs, 9 preamplifier supply (1.2V)



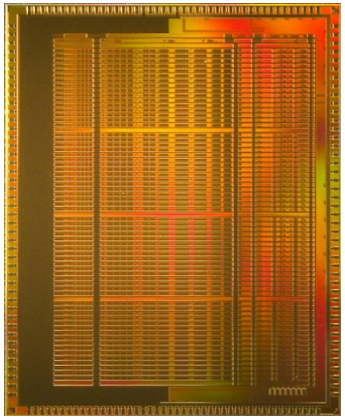
TGC outs 7-42

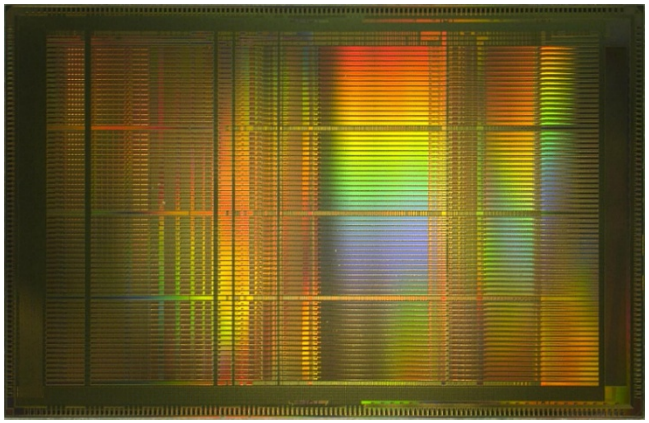
analog, mixed-signal, digital supplies (1.2V) – neighbor.bottom
– TGC outs 43-63

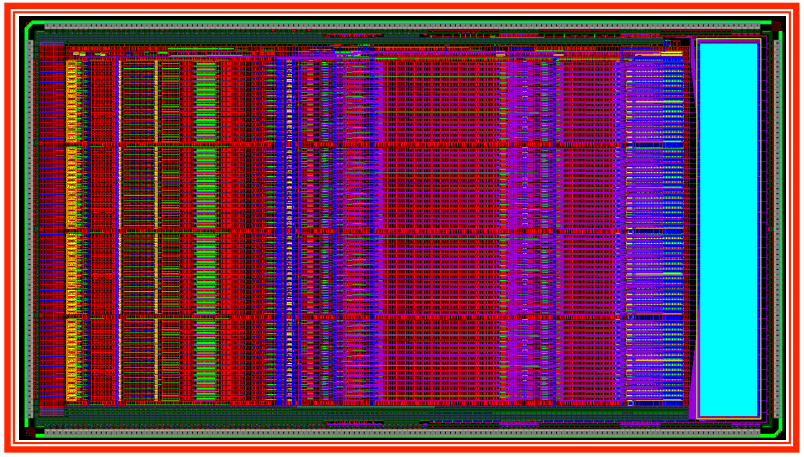
13.5 mm

392 bonding pads

Front-end ASIC for Muon New Small Wheel (4)







VMM1 (2012)
50 mm²
500k MOSFETs (8k/ch.)
- mixed-signal
- 2-phase readout

VMM2 (2014)
115 mm²
> 5M MOSFETs (>80k/ch.)
- planned deep re-design of VMM1
- much higher functionality and complexity than VMM1
- continuous fully-digital readout

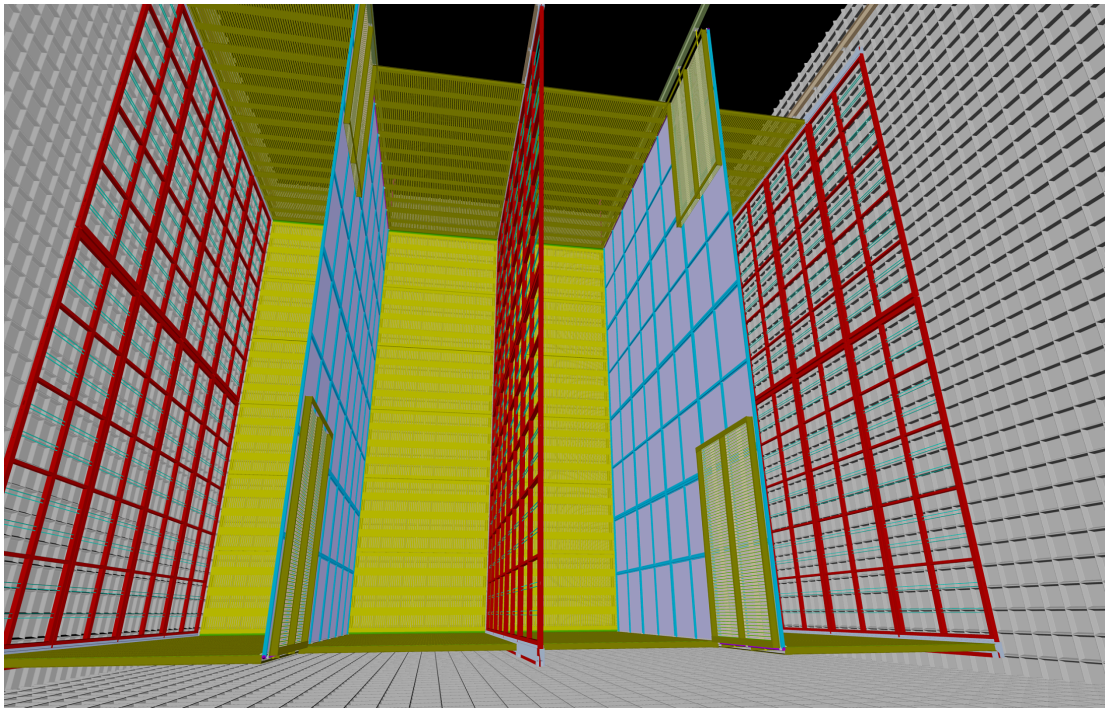
VMM3 (2015-16)
130 mm²
> 6M MOSFETs
- **L0 handling, SEU-tolerant, SLVS IOs, deeply revised front-end for sTGC signals, various additional functions, various fixes**
- **input from many collaborating teams with broad range of expertise**
- **aims at pre-production**

- *VMM ASIC is a SoC developed for Muon NSW in ATLAS Phase-I upgrade*
- *Collaborating with university groups, study is ongoing to use VMM in MDT trigger and readout design in ATLAS Phase-II upgrade*

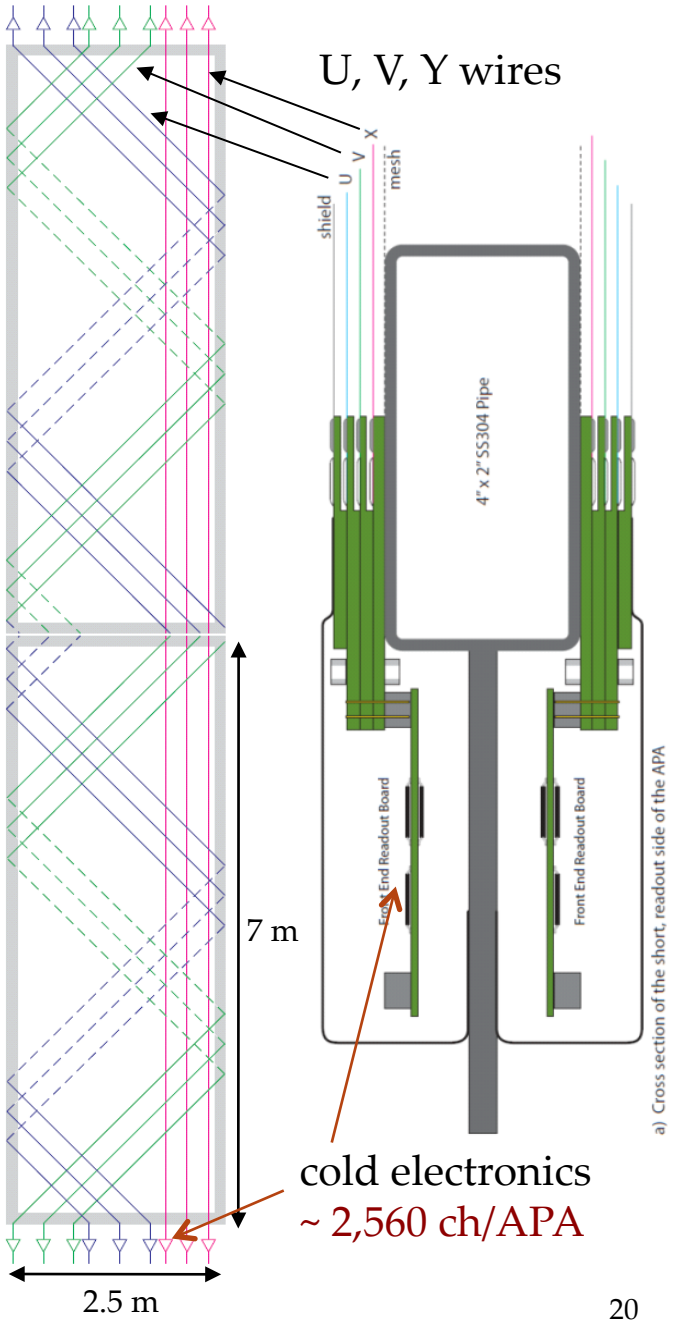
Future Plans

- Neutrino Experiment
  - DUNE Far Detector
- Hadron Collider Experiment
  - ATLAS Phase-II Upgrade
- ***Long term R&D is focused on the SoC (System on Chip) design***
  - Both DUNE and ATLAS Phase-II Upgrade will benefit from the highly integrated front end readout R&D
    - It has potential to instrument a greatly simplified detector readout system
    - It is long-term R&D with high risk and high return
  - Advancement of generic R&D enables the evolution of readout solution for both neutrino experiment and hadron collider experiment

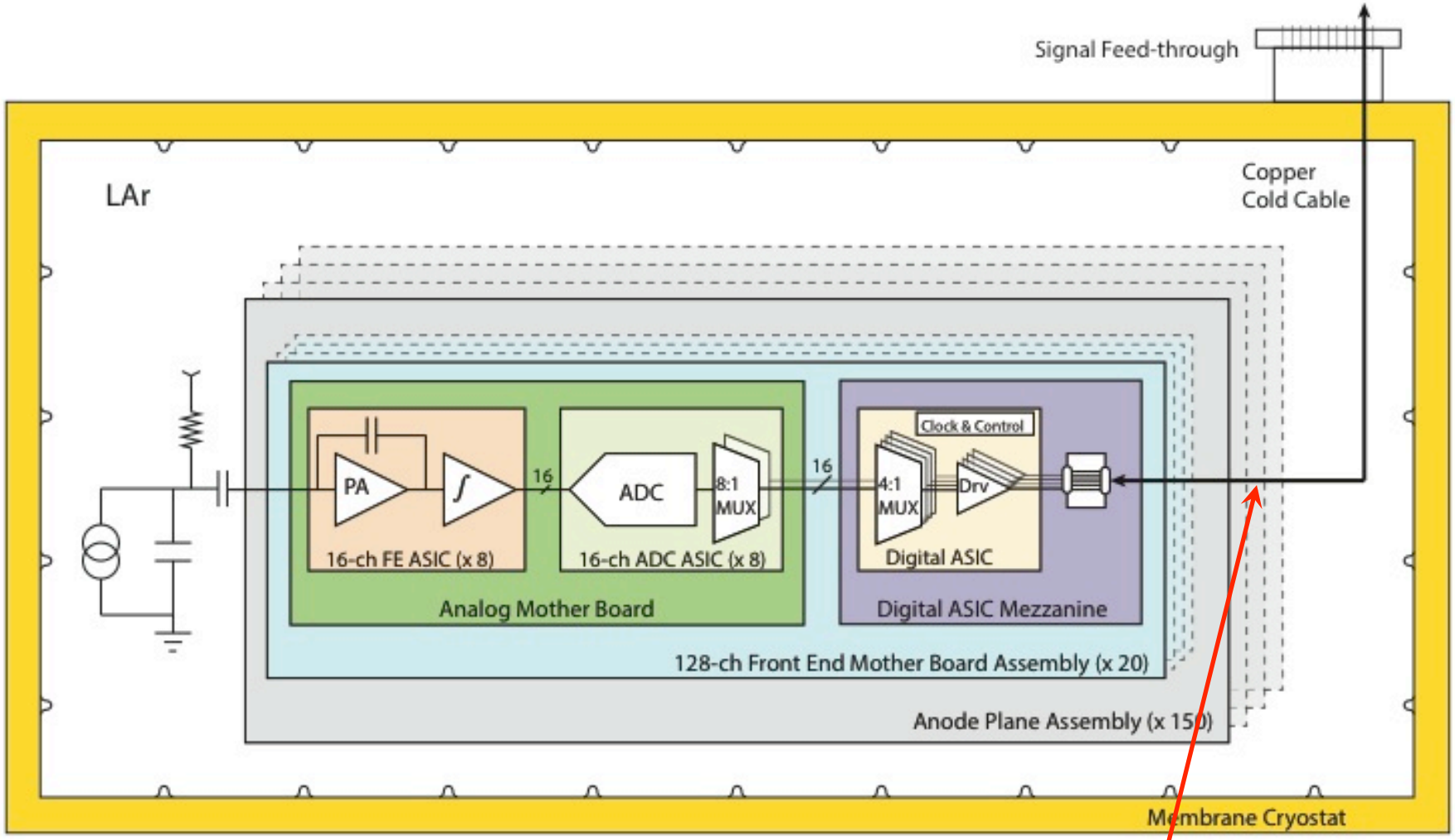
Cold Electronics for DUNE Far Detector



- BNL is developing APA & front end cold electronics system for DUNE far detector
- DUNE 10 kt Far Detector
  - ***384,000 channels***
  - 24,000 FE ASICs/24,000 ADC ASICs
  - 6,000 COLDATA ASICs (FNAL)
  - 3,000 Front End Mother Board assemblies

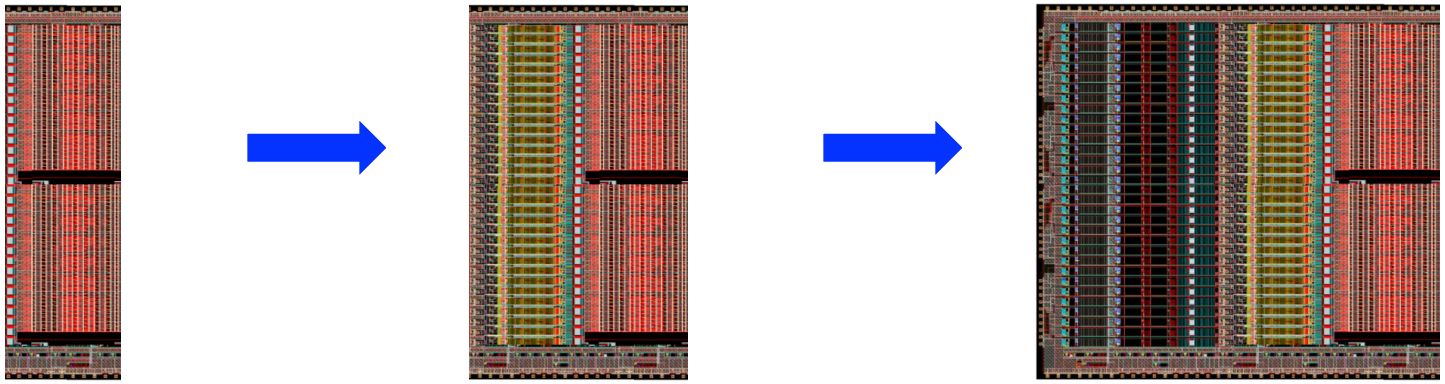


DUNE FD TPC Readout Electronics



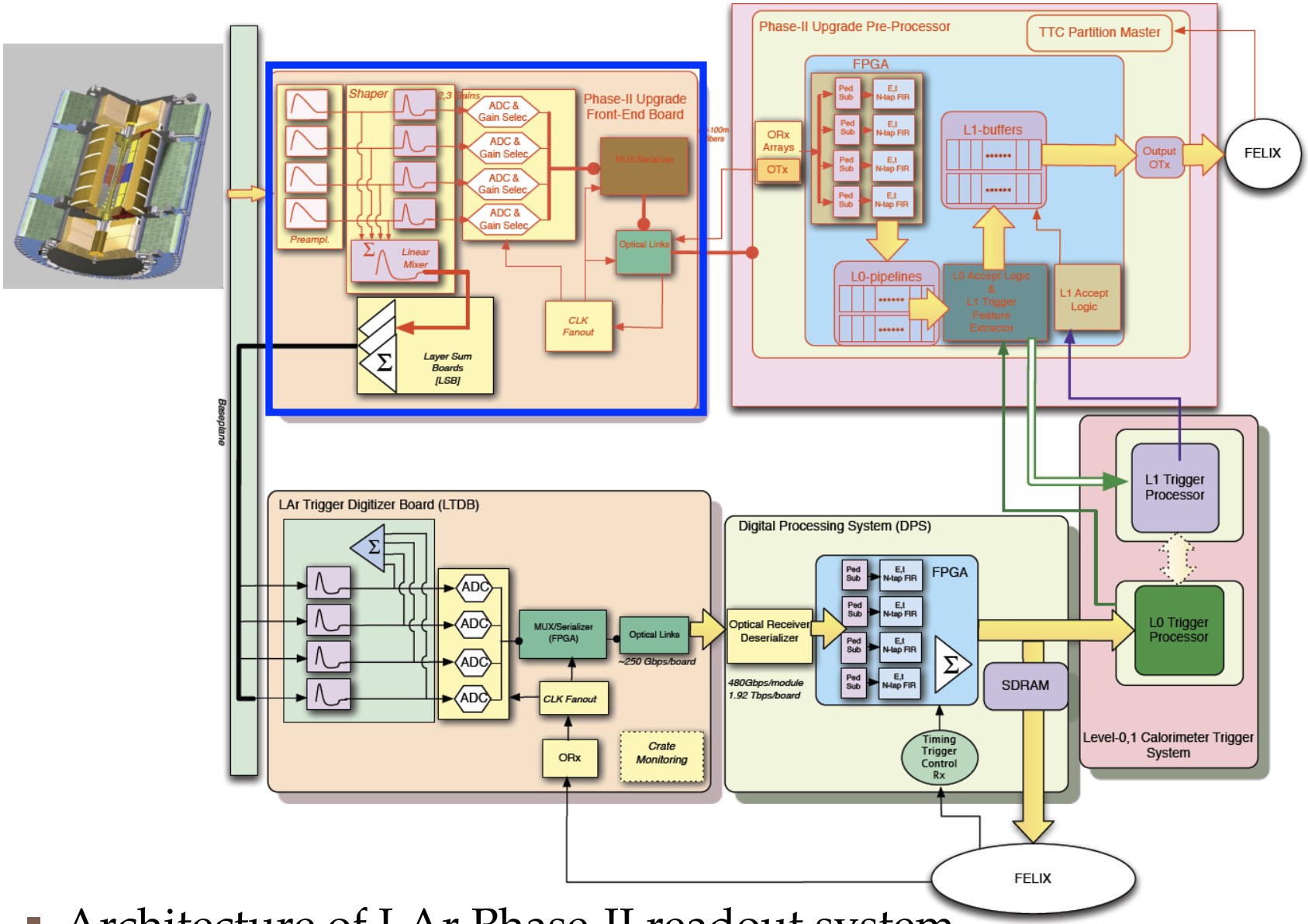
Fully Integrated Cold ASIC

- An R&D plan is to explore a development path to better optimized system
- A 32-channel fully integrated ASIC can be developed for LArTPC, it will have
  - 32-ch preamplifier and anti-alias shaper
  - 32-ch 2 MS/s 12-bit low power ADC
  - 1-ch serializer for data transmission @ 1 Gb/s
- This will be leveraging past development efforts and expertise from cold FE and ADC ASIC development since 2008
  - ADC ASIC that was developed is not just a simple multi-channel ADC, but it also provides S/H at the input and buffering, multiplexing and serialization at the output
  - The multiplexing degree and channel number can also be increased, if the application requires
- A full integrated ASIC opens the door to other possibilities, can be used in many other experiments (e.g. $0\upsilon\beta\beta$ experiment nEXO for charge readout)
  - ***From generic R&D evolving into customized solution for various particular experiments***



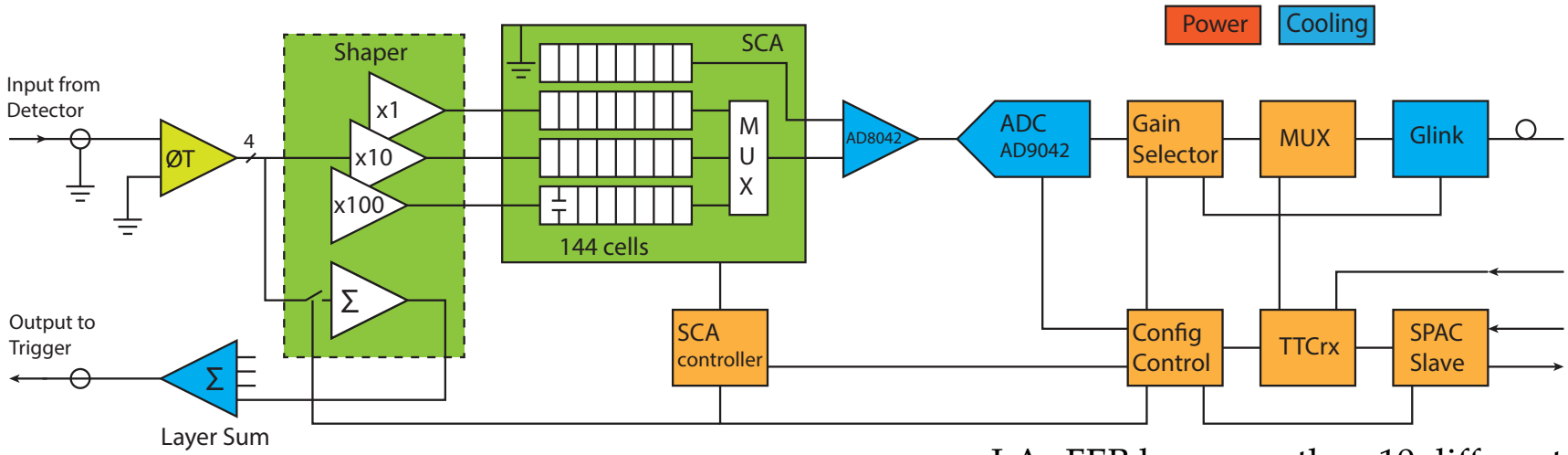
Develop PLL and serial link → 32-ch ADC with PLL and serial link → Fully integrated 32-ch cold ASIC

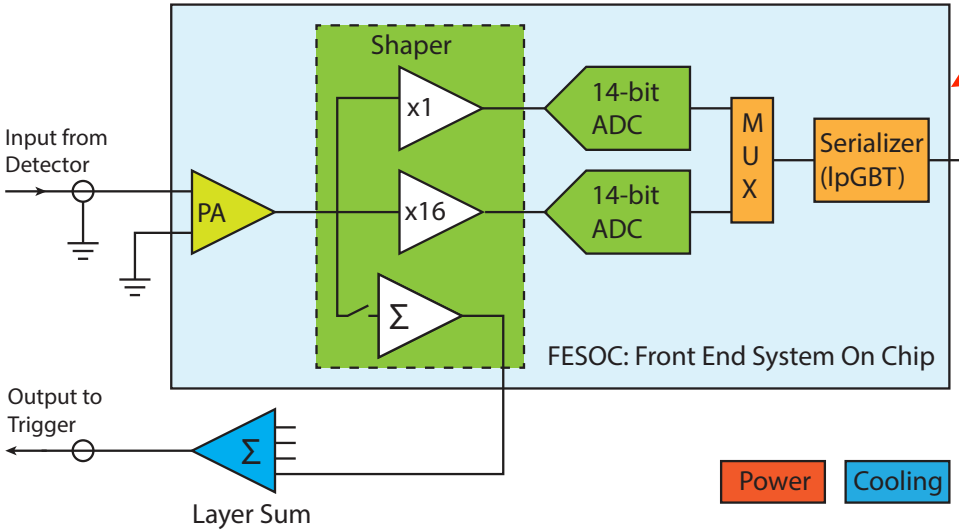
LAr Phase-II Upgrade



- Architecture of LAr Phase-II readout system

From LAr FEB to FEB-2





- LAr FEB has more than 10 different ASICs designed in 4 different technologies
  - *Can we do better in Phase-II upgrade?*
- FESOC (Front End System on Chip) in 65nm CMOS technology
- FESOC will greatly simplify the design of FEB-2, and ease the system power and cooling management
- Will first demonstrate analog front-end with satisfactory performance
  - Followed by the integration of 12-bit/14-bit ADC on chip
  - Final FESOC will use lpGBTx IP core currently being developed at CERN

Collaboration With Universities

- *P5 Recommendation 28: Strengthen university-national laboratory partnerships in instrumentation R&D through investment in instrumentation at universities. Encourage graduate programs with a focus on instrumentation education at HEP supported universities and labs, and fully exploit the unique capabilities and facilities offered at each.*
- Collaboration universities
  - Neutrino experiments
    - Bern, Chicago, Cincinnati, Columbia, MSU, Penn, SMU, Syracuse, UT Arlington, Yale
  - ATLAS detector upgrade
    - Arizona, NTU Athens, Chicago, Columbia, Harvard, Indiana, Penn, Pittsburgh, SMU, Stony Brook, UT Dallas, Yale

Resources & Budget

- KA25 support on integrated detector readout R&D
  - Francesco Lanni (0.25 FTE) in Physics Department
  - ASIC Design Engineer (0.33 FTE) in Instrumentation Division
- Budget
  - Besides KA25 support, the R&D effort of integrated detector readout is mainly supported by near term, high priority projects
    - This is well aligned with P5 recommendation
    - ***However this is competing with other R&D efforts***
  - Long term R&D (e.g. Cold Electronics, System on Chip) effort has limited support on KA25
    - Additional support is crucial for long term R&D
    - ***Request additional support of 1 FTE to strength the R&D effort***

Conclusion

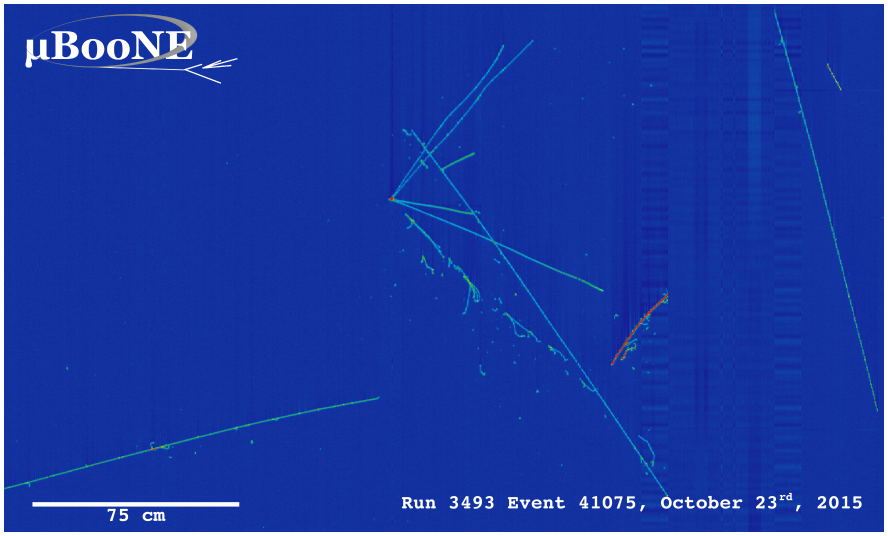
- ***R&D of integrated detector readout at BNL has been focused on the overall system optimization for experiments***
  - Front-end ASIC design is optimized for detector technologies
  - Front-end board design is tailored for experimental environment (radiation, cryogenic temperature etc.)
  - Trigger/DAQ design explores the ultimate use of COTS solution (high speed optical link, DSP in FPGA etc.)
- ***Detector R&D has developed expertise at BNL to provide an integrated solution of readout system for future experiments***
  - It is well aligned with P5 recommendation
  - A recent example is the readout system for SBND at Fermilab and protoDUNE at CERN → ***short-term high priority project***
  - R&D in FESOC of ATLAS Phase-II Upgrade and Full Integrated Cold ASIC for TPC readout → ***long-term R&D with high risk and high return***

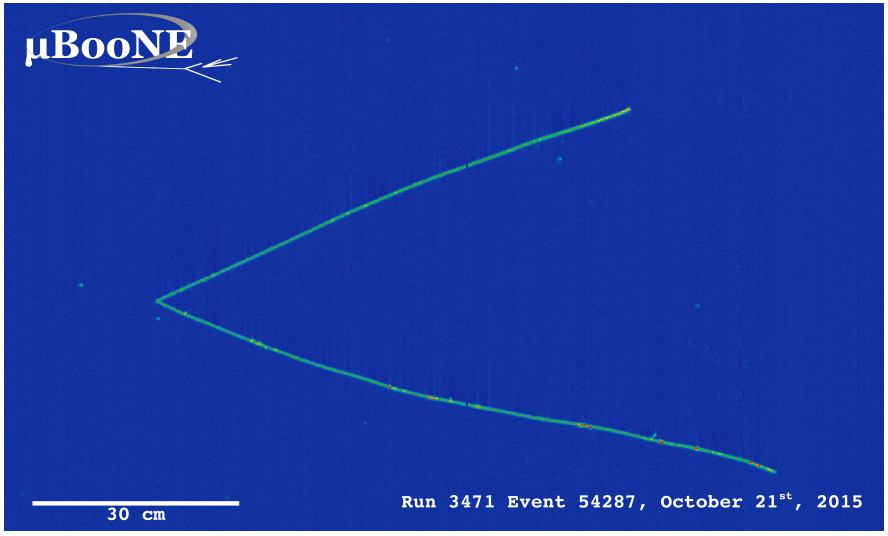
Backup Slides

Summary – Hadron Collider Experiment

- LAr Calorimeter Trigger Electronics in Phase-I ATLAS Upgrade
  - ~40,000 super cell signals, digitized on detector with high speed, low power, rad-hard ADC
  - ~25TeraBit/s of data is streamed out of detector continuously through parallel fiber optical links
  - High speed, real time, parallel digital signal processing in modern FPGA for calorimeter trigger generation
- New Small μ-Wheel in Phase-I ATLAS Upgrade
  - Front end chip with versatile functionalities to meet different detector technologies (both Micromegas and sTGC)
  - On chip charge and time digitization, buffering and multiplexing into a high speed serial link
  - Industry standard link interface to connect directly to a computer eliminating any additional conventional DAQ hardware
- Trigger/DAQ System in Phase-I ATLAS Upgrade
  - A single module with high density optical transmission and parallel DSP in FPGA to process whole ATLAS calorimeter information to produce large-R jet trigger
  - Innovative DAQ platform based on high speed parallel fiber optical link and PCIe Gen3 hardware to eliminate conventional DAQ hardware
- ATLAS LAr Phase-II Upgrade
  - Development of front end electronics will focus on 65nm based FESOC
  - Will greatly simplify the system design and overall power management

Summary – Readout of Noble Liquid TPCs



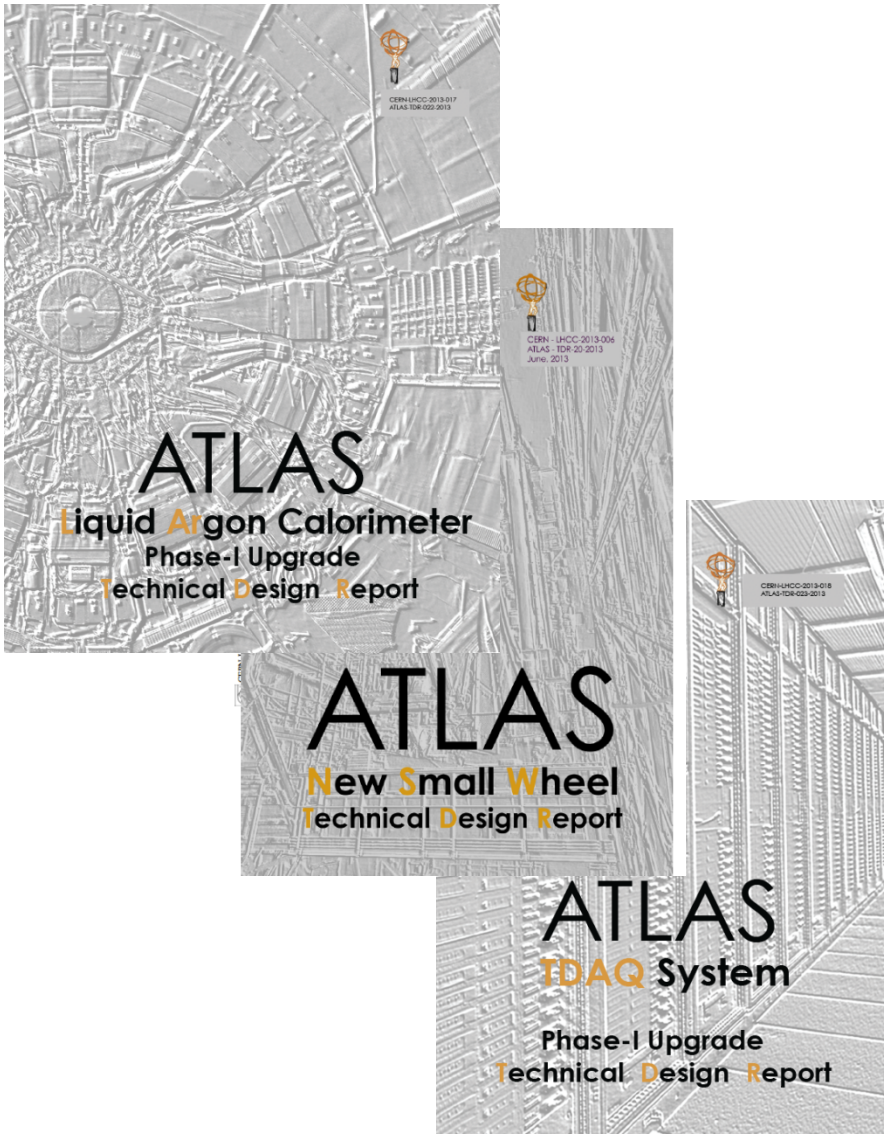


- Readout electronics developed at BNL for low temperatures (77K-300K) is an ***enabling*** technology for noble liquid and mixed phase detectors for neutrino and dark matter research.
- Cold electronics decouples the electrode and cryostat design from the readout design. With electronics integral with detector electrodes the noise is independent of the fiducial volume (signal cable lengths), and much lower than with warm electronics.
- Signal ***multiplexing*** results in large reduction in the quantity of cables (less outgassing) and the number of feedthroughs/cryostat penetrations.
- MicroBooNE is the first running experiment instrumented with CMOS cold electronics
- Full cold readout chain with FE ASIC, ADC ASIC and FPGA/COLDAT will be used to equip the SBND and DUNE LAr TPC

Integrated Readout and Trigger/DAQ System

- With deep submicron technology (130 nm, or less) the ADC and powerful DSP processing can be integrated with the low noise front end to a greater extent than ever before
- Front-end optimized for each of different detector technologies
  - Low noise, low power analog front end: preamplifer, shaper etc.
- Analog-to-Digital Converters
  - Low power, high resolution and high density
- FPGA
  - FPGA (also for operation in LAr) with flexible algorithms for data processing and reduction
- Data Link
  - High speed serial link to unify the interface to back end system
  - It simplifies the interface to DAQ PC farm, minimizes or eliminates the conventional DAQ hardware

ATLAS Phase-I Upgrade

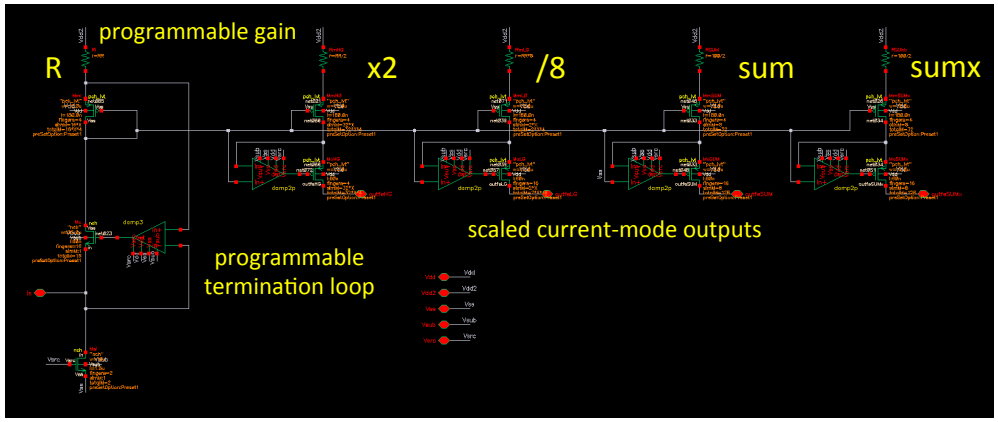


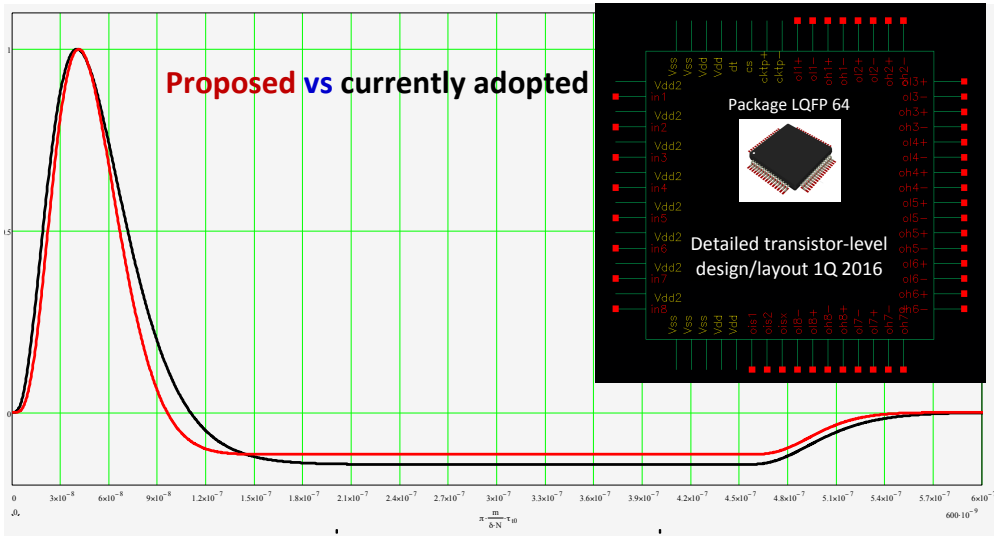
- BNL is actively involved in the ATLAS Phase-I upgrade
- BNL is a main contributor to all of three subsystems in Phase-I Upgrade
  - *Liquid Argon Calorimeter*
  - *Muon New Small Wheel*
  - *TDAQ System*

Motivations for Front-End System-on-Chip (FESOC)

- FESOC will greatly simplify the design of FEB-2
  - Evaluation of FESOC will serve the purpose of prototype development of FEB-2
  - Full solution of FEB-2 will be gradually developed along FESOC development, from board design, power and cooling design, system integration to final production and installation
  - Limited R&D in early FYs is required for FEB-2 design and integration
- The main FEB-2 development will focus on chip level integration instead of board level integration
- FESOC will reduce the power consumption significantly
  - Will ease the system design, including LVPS and cooling
- 65nm CMOS is a potentially viable solution for FESOC
  - Need to demonstrate analog front-end with satisfactory performance
  - A few on-going developments for ADC
  - lpGBTx is being developed in 65nm CMOS at CERN

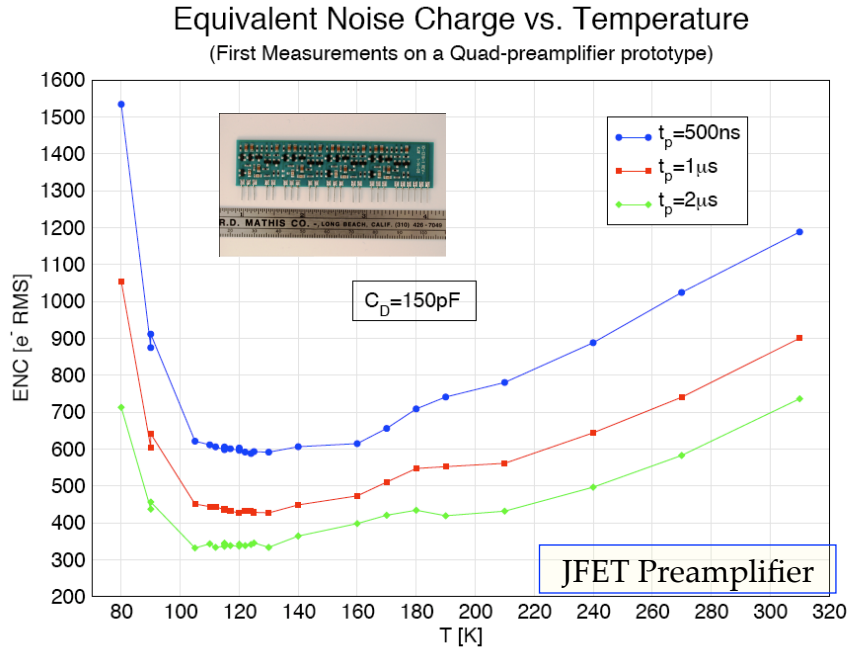
R&D of Front-End System-on-Chip (FESOC)

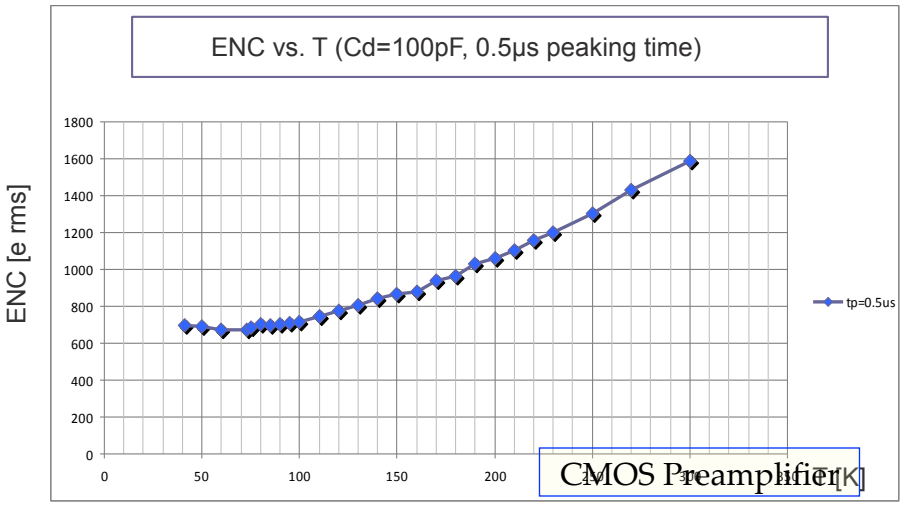




- FESOC will greatly simplify the design of FEB-2
  - The main FEB-2 development will focus on chip level integration
  - FESOC will reduce the power consumption significantly, ease the system power and cooling management
- 65nm CMOS is a potentially viable solution for FESOC
  - Unbalanced differential amplifier with programmable gain/termination, and high-order programmable anti-aliasing filters
  - At equal peaking time offers smaller tail and faster return to baseline, thus lower the pile-up
- Will first demonstrate analog front-end with satisfactory performance
  - Following by the integration of 12-bit/14-bit ADC on chip
  - Final FESOC will use lpGBTx IP core currently being developed at CERN

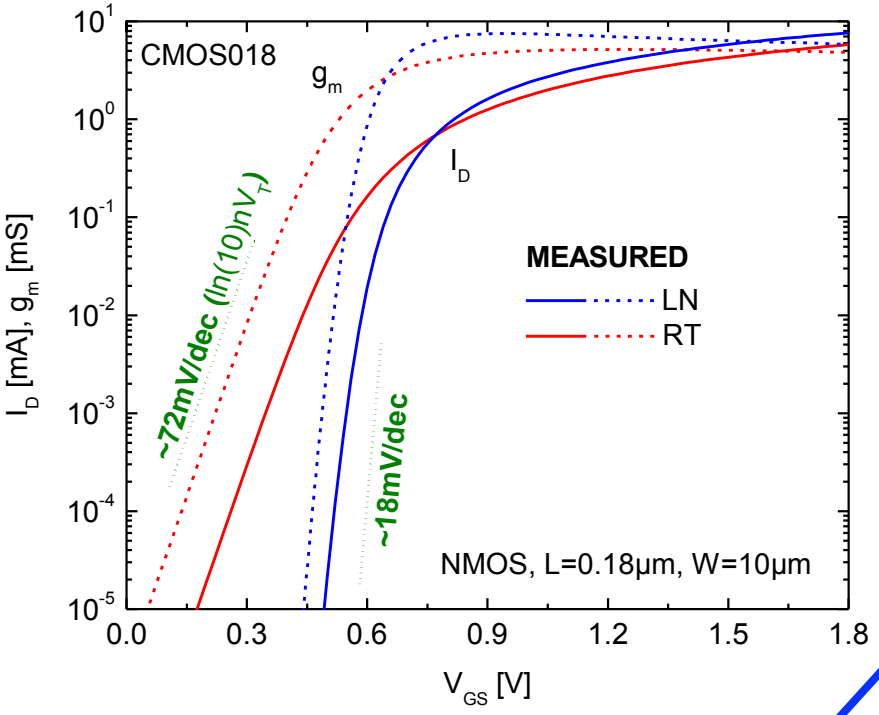
Cold Electronics: From JFET to CMOS

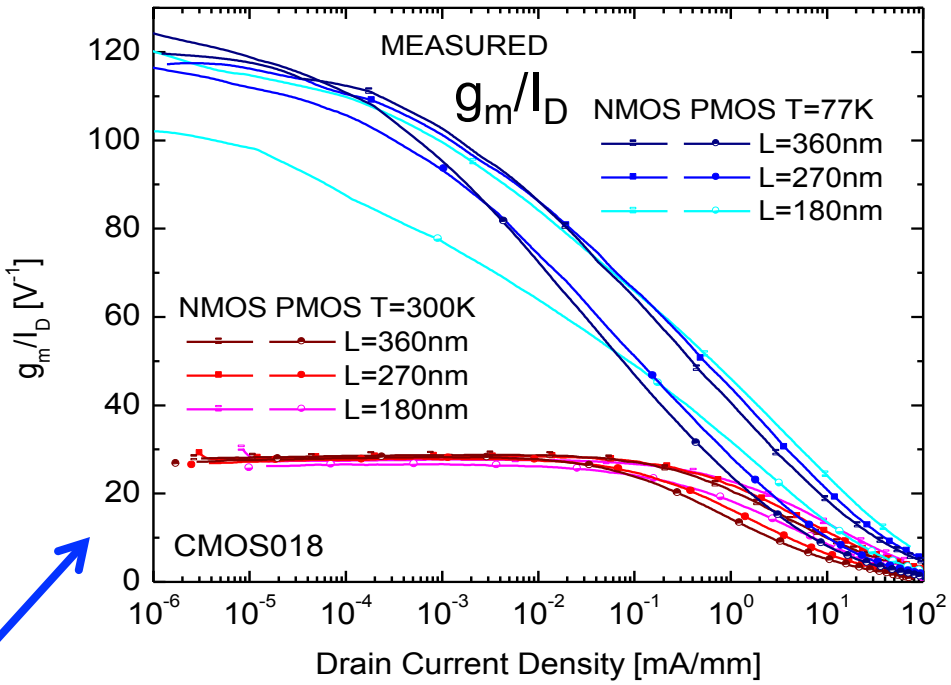




- BNL has a long history of development of cold electronics
  - NA34/HEILOS, NA48/NA62
- JFET based preamplifier designed for MicroBooNE
  - Bulk mobility and transconductance increase as temperature decreases, carrier freeze out causes ENC increasing when temperature lower than ~100K
- CMOS technology – test result of an existing ASIC in 0.25 *μm (not designed for LAr)*
  - CMOS in LAr has less than half the noise as that at room temperature, higher mobility and higher transconductance/current ratio
- MicroBooNE has adopted the cryogenic CMOS analog front end ASIC developed for DUNE LAr TPC program

CMOS Characteristics in LAr



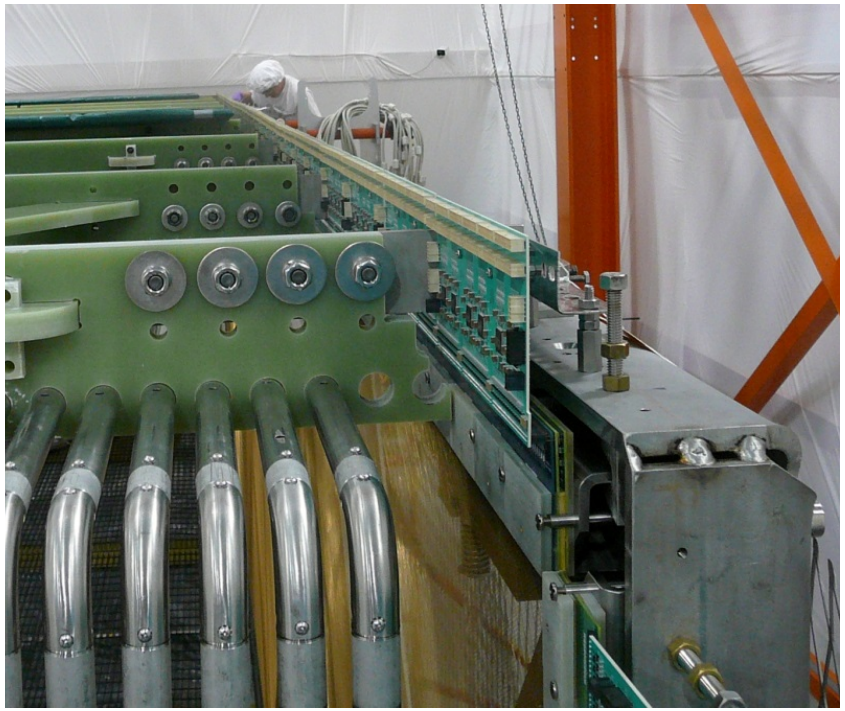


Transconductance/ drain current

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \ \ at \ \ T = 300K \\ \sim 116 \ \ at \ \ T = 77K \end{cases}$$

At 77-89K, charge carrier ***mobility*** in silicon *increases* and ***thermal fluctuations*** *decrease* with ***kT/e***, resulting in a ***higher gain***, ***higher*** g_m/I_D, ***higher speed*** and ***lower noise***.

MicroBooNE Front-end Electronics (3)

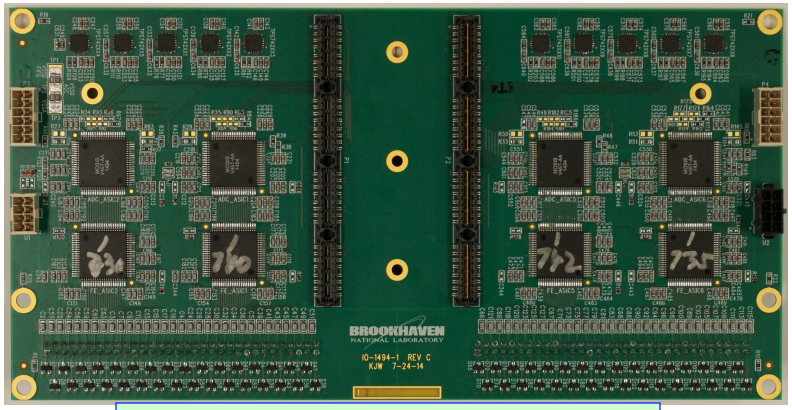


- **50 cold mother boards (8,256 channels)** are installed on MicroBooNE TPC, all channels tested successfully
- The full chain of front-end readout electronics has been installed in cryostat and tested successfully in January 2014
- Detector has been moved to experimental hall in June 2014

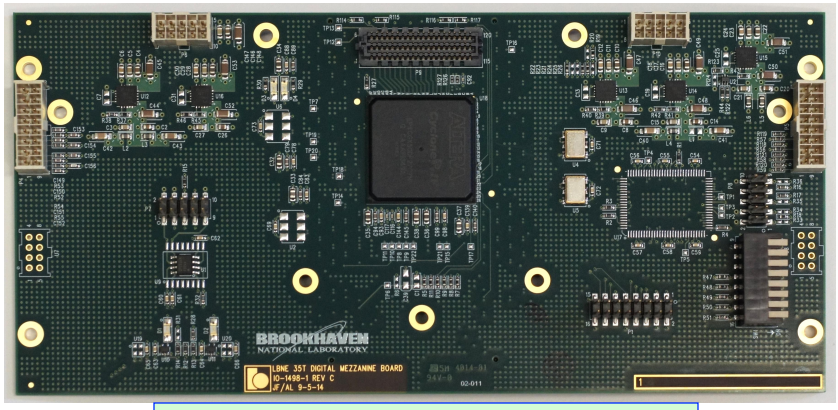
SBND/DUNE Front-end Electronics

- Readout chain ASICs are integrated with the TPC electrodes in LAr to minimize the capacitance and noise
- On chip **digitization** to convert to digital signals inside detector cryostat
- **Multiplexing** to high speed serial link, to reduce cable plants, minimize outgassing, make possible the scalability to larger detector volumes
- **Cold FPGA** to house the flexible algorithms for data processing and data reduction
  - An important component for near term project before digital ASIC becomes available
- Industry standard serial link interface to connect directly to back end system minimizing conventional DAQ hardware

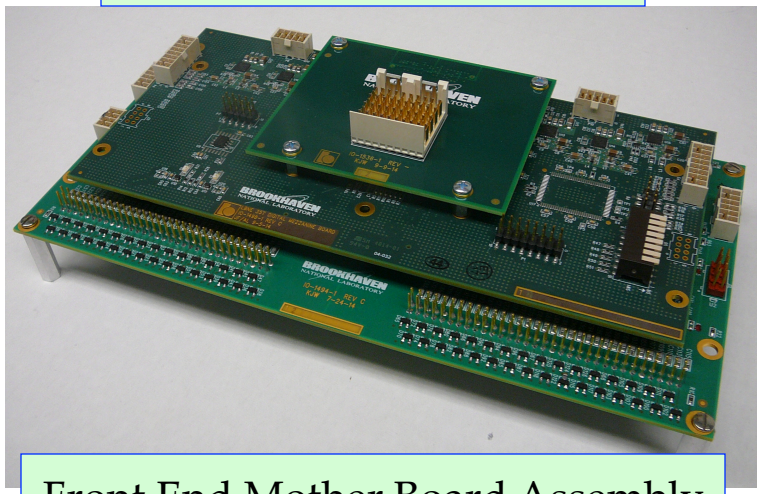
DUNE 35 Ton Cold Electronics – Basis of SBND/ DUNE FEMB Design



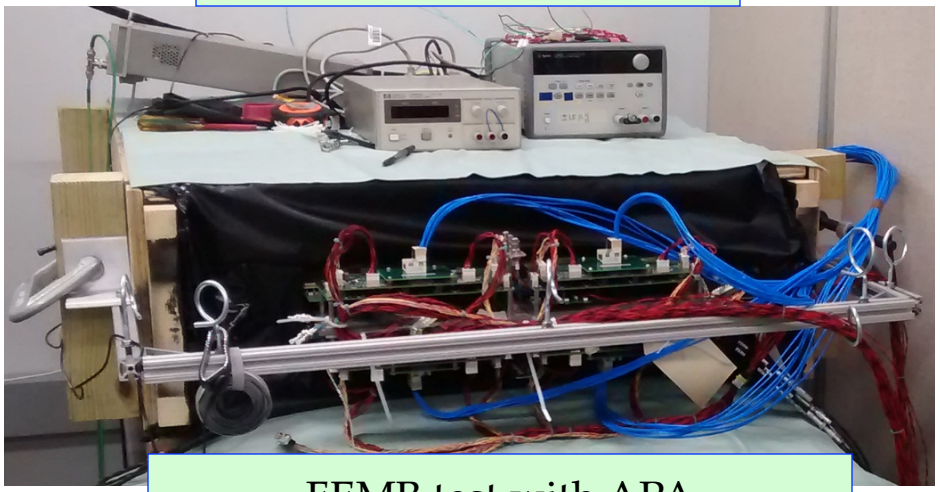
Analog Mother Board



FPGA Mezzanine



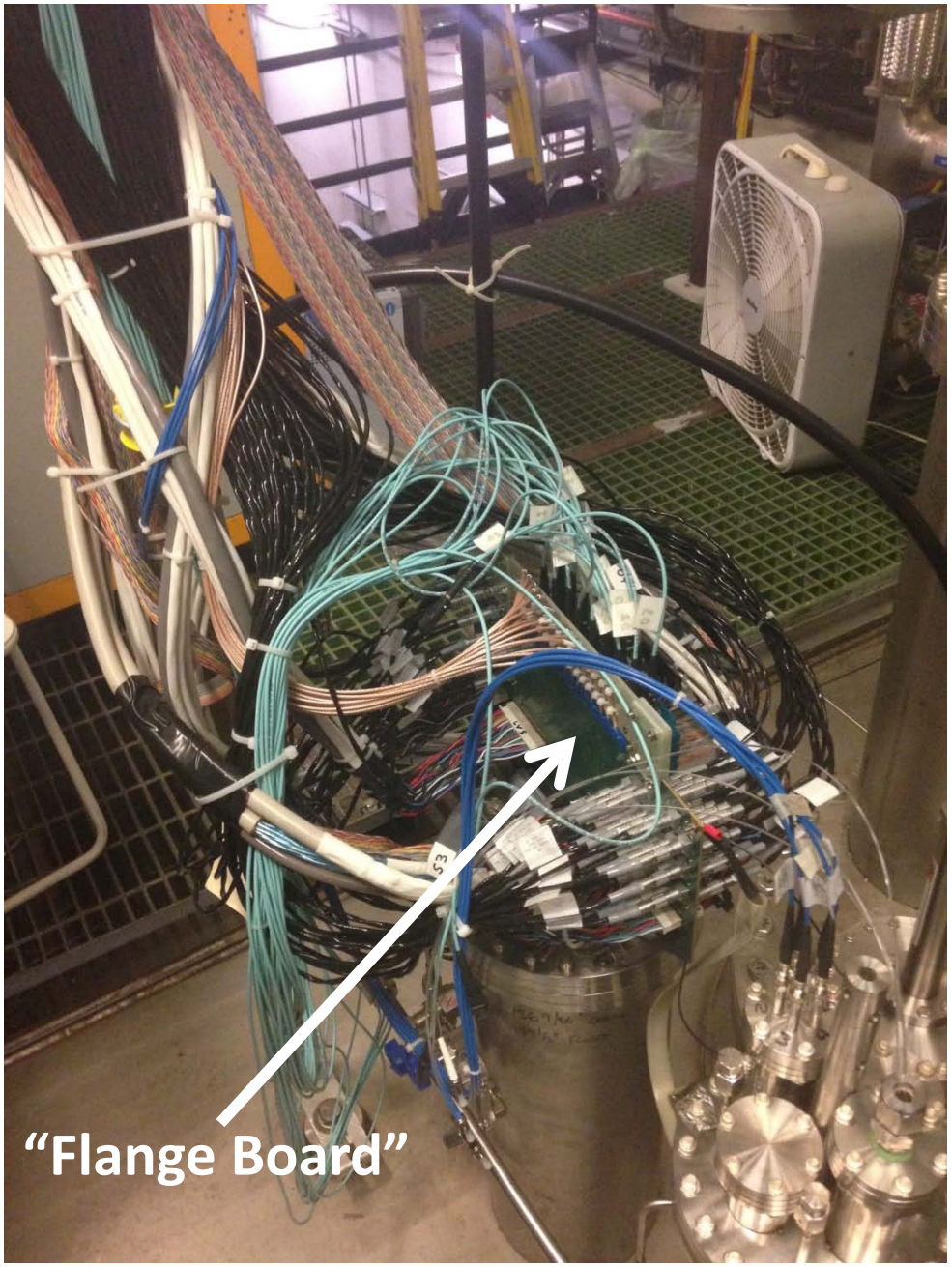
Front End Mother Board Assembly



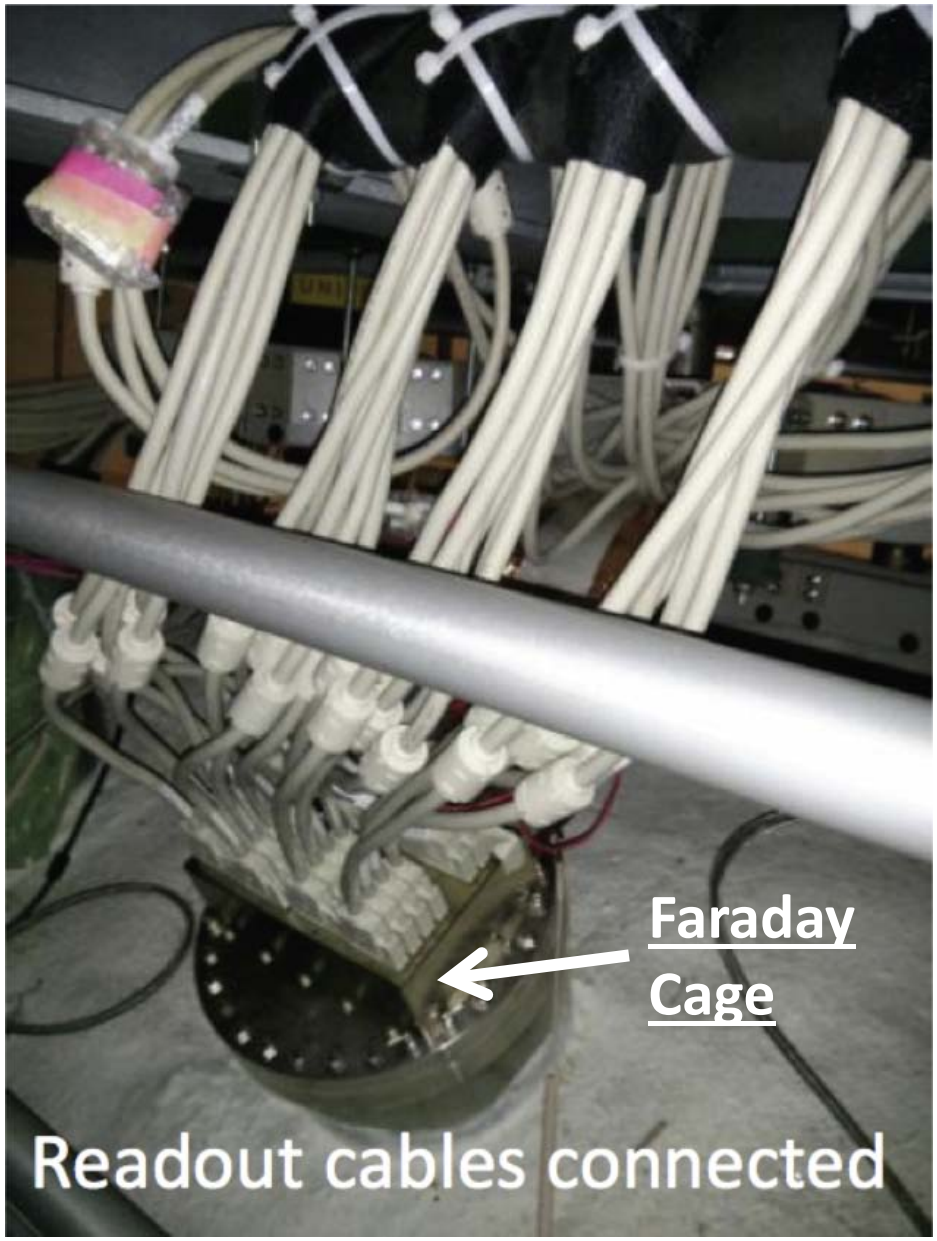
FEMB test with APA

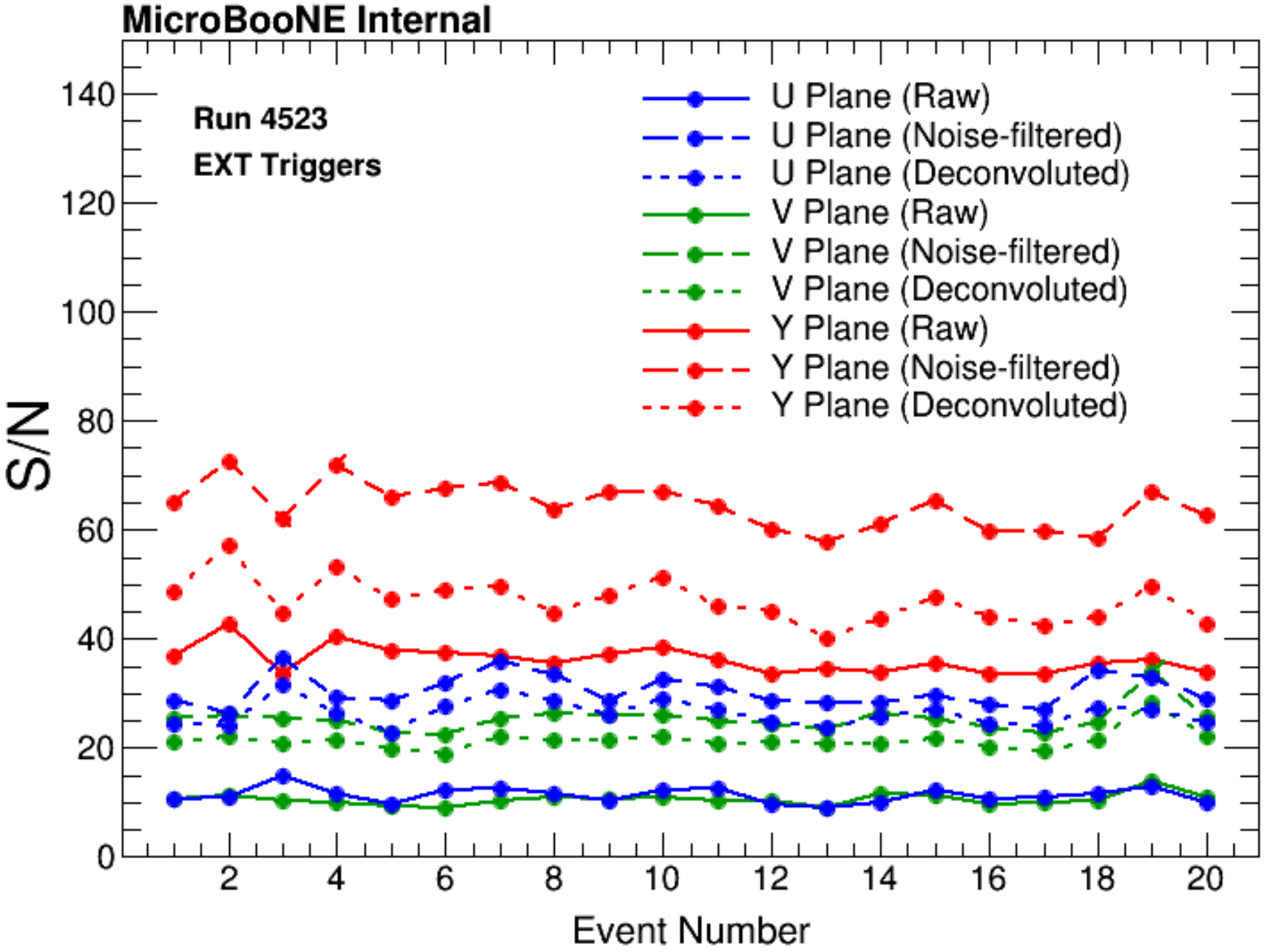
- DUNE 35 ton operation is ongoing

35ton (open) feedthrough



MB feedthrough




MicroBooNE Internal
Run 4523
EXT Triggers
U Plane (Raw)
U Plane (Noise-filtered)
U Plane (Deconvoluted)
V Plane (Raw)
V Plane (Noise-filtered)
V Plane (Deconvoluted)
Y Plane (Raw)
Y Plane (Noise-filtered)
Y Plane (Deconvoluted)
S/N
Event Number
0
20
40
60
80
100
120
140
2
4
6
8
10
12
14
16
18
20